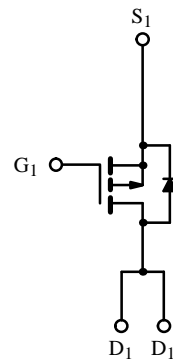
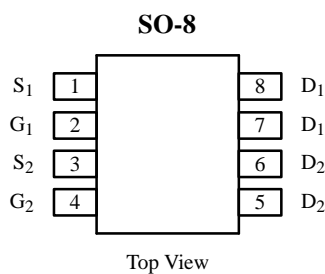


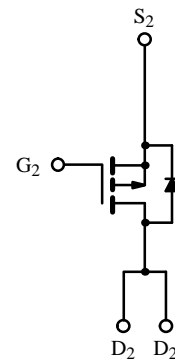
**Dual P-Channel Enhancement-Mode MOSFET**

**Product Summary**

$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
-60	0.28 @ $V_{GS} = -10$ V	$\pm 2.0$
	0.50 @ $V_{GS} = -4.5$ V	$\pm 1.6$



P-Channel MOSFET



P-Channel MOSFET

**Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$  Unless Otherwise Noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	$\pm 2.0$
		$T_A = 70^\circ\text{C}$	$\pm 1.6$
Pulsed Drain Current	$I_{DM}$	$\pm 10$	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	-2.0	
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	2.0
		$T_A = 70^\circ\text{C}$	1.3
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

**Thermal Resistance Ratings**

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board,  $t \leq 10$  sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70135. A SPICE Model data sheet is available for this product (FaxBack document #70517).

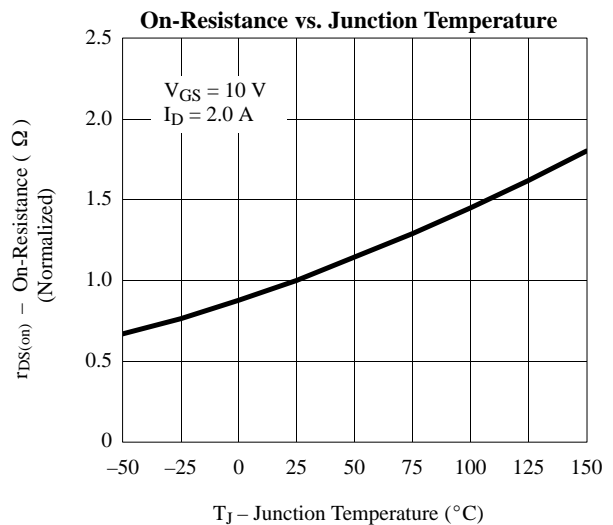
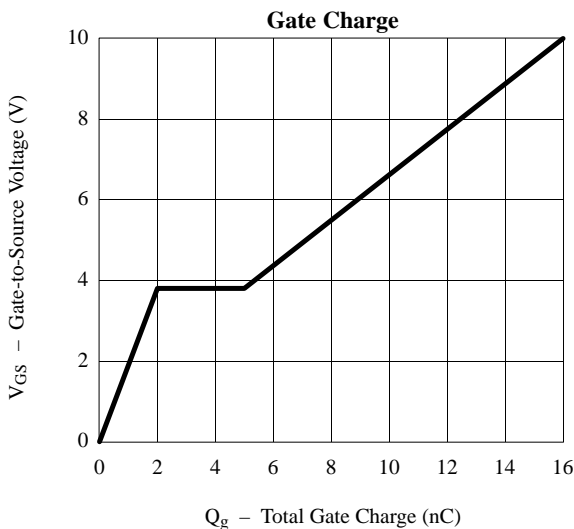
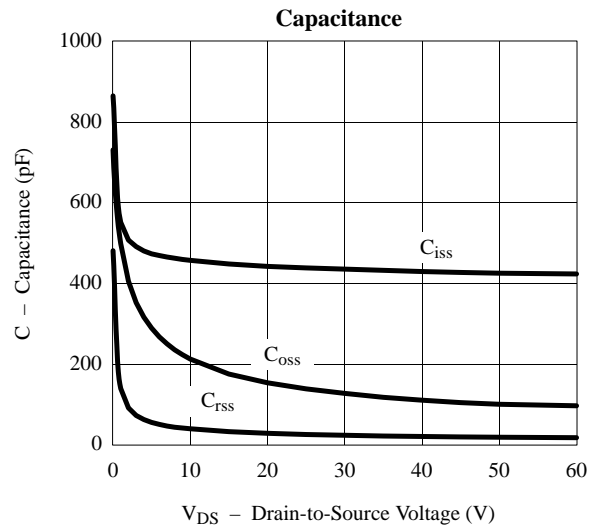
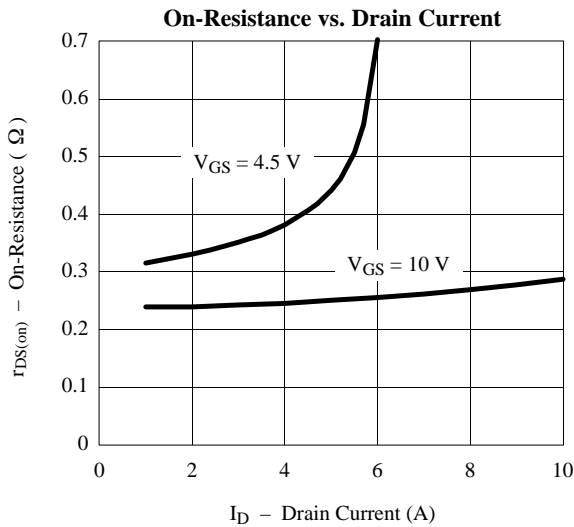
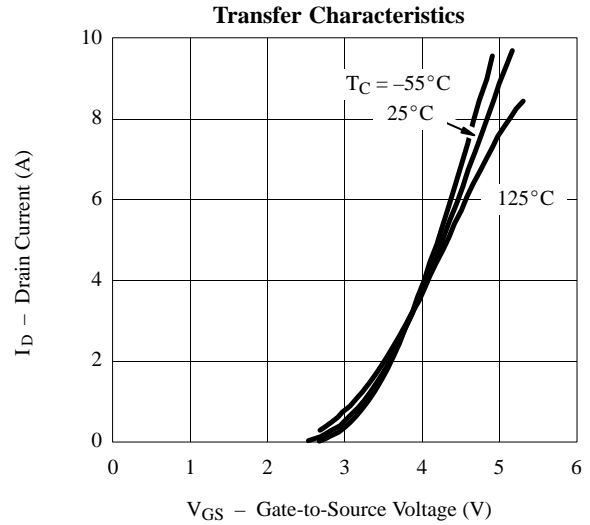
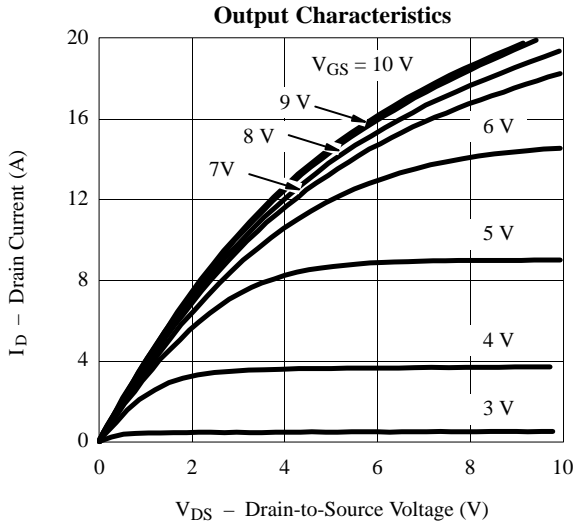
**Specifications ( $T_J = 25^\circ\text{C}$  Unless Otherwise Noted)**

Parameter	Symbol	Test Condition	Min	Typ <sup>a</sup>	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-1			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -40 \text{ V}, V_{GS} = 0 \text{ V}$			-2	$\mu\text{A}$
		$V_{DS} = -40 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			-25	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} \leq -5 \text{ V}, V_{GS} = -10 \text{ V}$	-10			A
Drain-Source On-State Resistance <sup>b</sup>	$r_{DS(on)}$	$V_{GS} = -10 \text{ V}, I_D = -2.0 \text{ A}$			0.28	$\Omega$
		$V_{GS} = -4.5 \text{ V}, I_D = -1.6 \text{ A}$			0.50	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = -15 \text{ V}, I_D = -2.0 \text{ A}$		5.0		S
Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$I_S = -2.0 \text{ A}, V_{GS} = 0 \text{ V}$		-0.9	-1.2	V
<b>Dynamic<sup>a</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = -30 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -2.0 \text{ A}$		16	30	nC
Gate-Source Charge	$Q_{gs}$			2.0		
Gate-Drain Charge	$Q_{gd}$			3		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -30 \text{ V}, R_L = 30 \Omega$ $I_D \cong -1 \text{ A}, V_{GEN} = -10 \text{ V}, R_G = 6 \Omega$		8	25	ns
Rise Time	$t_r$			11	30	
Turn-Off Delay Time	$t_{d(off)}$			28	60	
Fall Time	$t_f$			14	40	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = -2.0 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		65	100	

## Notes

- a. Guaranteed by design, not subject to production testing.  
 b. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .

**Typical Characteristics (25°C Unless Otherwise Noted)**



## Typical Characteristics (25°C Unless Otherwise Noted)

